TECHNISCHE UNIVERSITÄT DARMSTADT

Geometry/Topology Optimization in High End Lithography

Proposal for a Master thesis or Internship @ ZEISS SMT GmbH
Study field: Computational Engineering | Computer Science | Electrical Engineering | Mathematics

Description

This research project is planned in cooperation with Carl Zeiss SMT GmbH, the Semiconductor Manufacturing Technology business group of ZEISS. Nowadays, most high-end microchips are produced using EUV-Lithography, where a design from a photomask is repeatedly printed on a wafer. Due to the electrodynamic light matter interaction, the photomask design and the corresponding image on the wafer may differ significantly. The goal of this thesis is the formulation, development, and benchmarking of a top-notch topology optimization solution solving inverse problems.

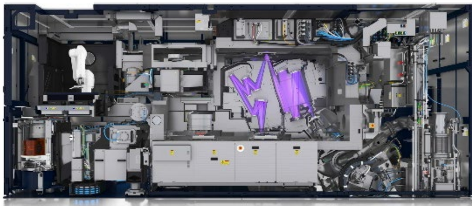

Figure 1: EUV Lithography.
Source: https://www.asml.com/en/products/euv-lithography-systems

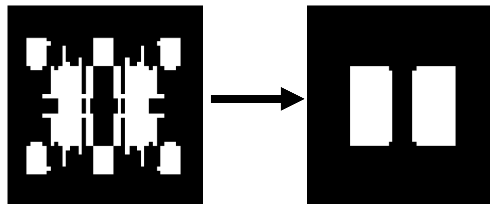

Figure 2: Mapping (forward simulation) from optimization domain (left) to target domain (right).
Illustration based on [Ma and Gonzalo. *Computational Lithography*, 2011.]

Work plan

- Literature study, identification of suitable approaches and methods
- Implementation of different optimization approaches
- Evaluation and comparison of methods
- Documentation and deployment in product

Prerequisites

- Numerical methods/optimization and programming in python

Contact:

Armin Galetzka
TEMF, TU Darmstadt
galetzka@temf.tu-darmstadt.de

Prof. Herbert De Gersem
TEMF, TU Darmstadt
degersem@temf.tu-darmstadt.de

Dr. Nikolai Schmitt
Carl Zeiss SMT GmbH
nikolai.schmitt@zeiss.com

Dr. Niklas Georg
Carl Zeiss SMT GmbH
niklas.georg@zeiss.com