Master's Thesis (30CP) / Bachelor's Thesis (12CP) / Seminar B (6CP) - Adapting the HDL lab to a Digital-On-Top Design Flow

TECHNISCHE UNIVERSITÄT DARMSTADT

27. Mai 2025

Description

Viktor Weinelt, M.Sc.
viktor.weinelt@ies.tu-darmstadt.de
+49 6151 16-20254
Room: S306 | 345

The HDL lab offered at the IES gives students a deep understanding of digital IC design. The lections in this course are on RTL design, test-benching, synthesis, place, and route, and also SDF back annotated simulations. In the end, students have a functional fully digital chip. However, in the real world, nearly no chip is purely digital. Yet the integration of analog designs, such as an ADC into a digital-on-top design flow is so far missing in the HDL lab. The idea is to provide students with a fully designed ADC (Schematic, Layout), and let them run timing and layout abstraction to get the .lef and .lib files needed to integrate the analog ADC into the synthesis and place and route workflow. As a result, students would be able to gain a better understanding of the design of mainly digital mixed-signal ICs.

Tasks

Depending on the type of seminar or thesis your tasks will be a part or all of the following:

- You design the ADC, before verifying its functionality and running timing and layout abstraction.
- You perform Verilog annotation to annotate the behavioral Verilog module with timing information.
- You run synthesis and place and route including the analog design.
- You write and define tasks for students of the HDL lab.
- Finally, you can adapt the HDL lab script to include the new tasks.

Your Skillset

For Master students: You should have attended the AICD lab and thus have enough skills in the field of analog IC design. You should know about the topic of RTL design and the synthesis and place and route workflow. Ideally, you also attended the HDL lab.
For Bachelor students: If you want to take this topic as a bachelor's thesis you should know about the topic of analog IC design. (AICD/EIS or equal.) Interest in Electronics and IC design is necessary.
General: You need to be a highly motivated and independent working student who has already taken labs or seminars at our institute. Your grades in lectures relevant for this topic should be above average.