Master's Thesis (30CP) - Construction and Simulation of an In-Memory Capable CMOS SRAM Cell which Enables Immediate AND and OR operations

TECHNISCHE UNIVERSITÄT DARMSTADT

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Description

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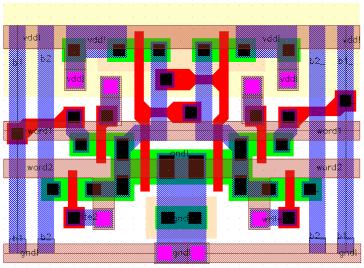
Modern data-centric applications, such as machine learning, neuronal networks and artificial intelligence (AI), are a significant challenge for today's computer industry. With the rising amount of data that has to be computed, the standard von Neumann Architecture comes to its limits. In the worst case, data must be passed from memory through several cache layers to the processing unit and back for each computational operation. As a result, latency significantly increases, decreasing the speed of computation. This issue is referred to as the "von Neumann bottleneck". In-memory computing is one approach to overcome latency related issues. By adding computational capabilities to the memory, data transfer to and from the memory cell can be minimised.



Tasks

Research in the topic of in-memory computing.
Development of a CMOS aproach that adds the computational capability for immediate AND and OR functions to an SRAM cell.
Layout and simulation of an array of the designed SRAM cells.
Writing a report in latex and presenting in front of a small audience in German or English.