Master Thesis: Short-Channel Multi-Decade Exponentiator and Logarithmizer in 28nm technology

TECHNISCHE UNIVERSITÄT DARMSTADT

Kurzkanal- Exponenzierer und Logarithmierer für mehrere Dekaden in 28nm-Technologie
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Description

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In this master thesis, a new circuit architecture for short-channel analog calculators will be explored.

Analog multiplication currently relies heavily on either square-law/sub-threshold MOSFET behaviour, or BJT characteristics. All of those possibilities come with significant area consumption and are not easily implementable in modern CMOS technology nodes. A new idea relies on approximating the exponential function with a finite-n chain of weakly nonlinear short-channel FET circuits, staying very close to its limit-value definition:

$$e^x = \lim_{n\to\infty}\left(1+\frac{x}{n}\right)^n \tag{1}$$

Furthermore, the proposed topology will allow for easy adaptation to logarithmic functions. A circuit exploiting this idea should be built and compared to literature in terms of accuracy, speed, size and power consumption. The usage of short-channel FETs offers significant advantages compared to other technologies. Size and therefore processing time can possibly be greatly reduced.

Now, what should be done?

- A thorough mathematical investigation of the circuit
- Development of a calibration strategy
- Schematic implementation, including reference and calibration circuitry
- Optimization for input bandwidth
- Layout design, Corner and Monte-Carlo Analysis

Requirements:

- Strong interest in non-linear system theory, bringing together mathematics and circuit design
- Some experience with Cadence
- Knowledge about analog circuit design
- Ability to solve problems and work independently

If you are interested in this topic, please feel free to ask questions!