Integrated Electronic Systems Lab
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TECHNISCHE UNIVERSITÄT DARMSTADT

Capacitance Modelling for Novel Reconfigurable FET

Proseminar/Projectseminar/Bachelorthesis

Description
A recently emerged device called planar RFET surpasses limitations of MOSFETs in ease of fabrication, temperature robustness and versatility. Being an ambipolar device the charge carrier type (electron or hole) is not determined at design time by placing either P-channel or N-channel devices. Instead an additional gate (backgate) allows for selection of the desired charge carrier type in an intrinsic channel. By controlling the backgate bias the planar RFET can either behave like an N-channel or a P-channel transistor. This can happen during operation of the IC, exposing an additional degree of freedom in circuit design.

While the existing DC bias model serves for DC simulations only, transient simulations require accurate capacitance modelling. Your task will be to analyze and model capacitances around the transistor model. You are free to find your own approaches e.g. through fitting/optimization, physical analysis or other methods. The planar RFET is subject of a publicly funded research project so that promising results are encouraged to be published in conferences or journals.

Prior knowledge in (some of) the following fields is beneficial:

- Semiconductors
- Spice simulators
- Python

Feel free to contact me for further information or seminar/thesis topics.

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