Integrated Electronic Systems Lab
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TECHNISCHE UNIVERSITÄT DARMSTADT

Seminar B

Custom Frequency Counter for a Chip Testing Platform

Description

We recently put a prototype of our chip in production and expect the delivery in a few months. To test the functionality and evaluate its performance, a test PCB will be designed. As part of the measurement process, the frequency of the integrated oscillators shall be measured. An FPGA is available on the test board. The design of such a measurement circuit is part of this seminar.

The oscillators of the chip will operate at frequencies between 50 – 300 MHz with low voltage levels. Signal conditioning is needed to ensure combability with standard CMOS logic levels. Furthermore, a clock prescaler might be needed, to generate a suitable frequency for interfacing with the FPGA. The FPGA-Board shall be used as core frequency counter. A resolution of 0.1 MHz or better shall be targeted.

The first task is to develop a suitable circuit based on off-the-shelf components. Components can be selected based on their datasheets, but unfortunately availability of these parts need to be considered. In case of severe shortage of parts, extensive support will be offered. Secondly, a small, minimal PCB with the developed circuit shall be designed and then tested in our laboratory. Lastly, the counting core should be implemented on an FPGA using Verilog and the overall system tested. Upon success we will incorporate the design on our test PCB for the chip.

Tasks

- Signal conditioning & prescaler circuit design
- Design of a minimal test PCB
- FPGA-based counter implementation in verilog

Requirements:

- Fundamentals of electronics
- Fundamental in verilog
- Experience in PCB Design is a plus

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