Master Thesis - One time programmable memory in 180nm technology

TECHNISCHE UNIVERSITÄT DARMSTADT

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Description

Low power non-volatile memory is an interesting area of research whenever one focuses on small and energy-efficient designs. It is important in the context of smart dust, but also plays a role for further applications, such as implants or RFID tags. One approach is the one time programmable memory (OTP), which in general stores information by destroying a device such as a capacitor or MOSFET on chip and therefore changing the device characteristic. There is a variety of OTP architectures in literature. The implementation includes a digital and analog part for simulation and therefore is a versatile task.

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Task

The task can include the development of a VerilogA model to simulate the break-down behaviour, designing a HV-switching structure, scaling the design up to 128bit memory and developing a Verilog controller. The design should be verified through simulations and ideally include a layout in the end.

Requirements

Good knowledge of Cadence and Verilog (f.ex. AICD-lab and HDL-lab)
Self organized and independent working style