Masterthesis:
All Digital Phase Locked Loop for Physical Memory Interface

TECHNISCHE UNIVERSITÄT DARMSTADT

Integrated Electronic Systems

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1 Introduction

The main task of the physical interface (PHY) is to connect dynamic random access memory (DRAM) devices with a memory controller (MC), as shown in Figure 1. Here, the PHY is responsible for data transmission and data reception. To achieve high transmission speeds, the clock used in the PHY needs to meet certain criteria. To fulfil ambitious clock constraints, Phase Locked Loops (PLLs) can be used, as they can be useful for several reasons:

- Synchronization: synchronize the clock signal between the MC, the PHY and the DRAM module
- Jitter reduction: reduce the amount of jitter (variation in the phase of the clock signal)
- Timing control: generate a clock signal that is used to control the timing of the memory accesses

The all-digital approach aims at technology-independence. With an implementation that is implemented in a Hardware Description Language (HDL) like Verilog, the all digital PLL (ADPLL) could be synthesised to many different technologies and thus, become reusable for different projects.

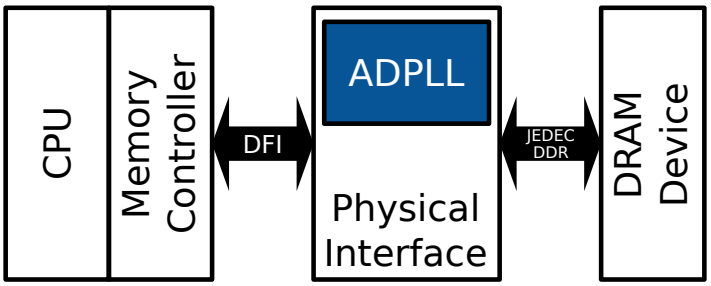

Figure 1: Schematic of an Memory System using a PHY with an ADPLL.

2 Tasks

The first task of this work is to do literature research on existing topologies of ADPLLs. In the subsequent task one of the topologies is implemented in Verilog and then synthesised to a netlist. The netlist is then layouted by an automated place-and-route tool afterwards. With the auto-generated layout, the device needs to be simulated in Cadence Virtuoso.

3 Required Skills / Courses

Experience with:

- Verilog or SystemVerilog is mandatory
- Synthesis (HDL Lab) is highly recommended
- Cadence Virtuoso is recommended