Design and Implementation of Equalizers using Adaptive Body Biasing in 22nm FDSOI Technology

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1 Description

As a master-level IC Designer, it is crucial to focus on achieving higher performance and lower power consumption, especially when operating at lower supply voltages (e.g., 0.8 V or less). Modern advancements in technology provide innovative techniques to address these challenges. One such technique is Adaptive Body Biasing (ABB), which dynamically adjusts the threshold voltage (V_{TH}) of MOSFETs in real time to optimize performance and power consumption based on specific operational needs. ABB includes two modes: Forward Body Biasing (FBB) and Reverse Body Biasing (RBB).

Forward Body Biasing (FBB) is a powerful method to enhance the performance of transistors in integrated circuits (ICs). It involves applying a bias voltage to the body terminal of a MOSFET, thereby modifying its threshold voltage and improving its drive strength and switching speed. In practice, FBB applies a voltage to the body terminal of a transistor that is opposite in polarity to the transistor type:

For n-type MOSFETs (NFETs): A positive voltage is applied to the body terminal. This reduces the threshold voltage (V_{TH}), allowing the transistor to conduct more easily, thereby improving performance.

For p-type MOSFETs (PFETs): A negative voltage is applied to achieve a similar effect, decreasing the threshold voltage and enhancing transistor performance.

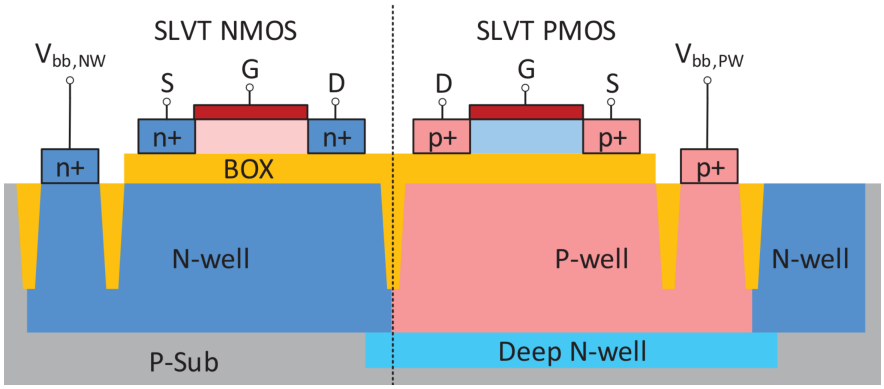

Figure 1: Structure of 22nm FDSOI technology.

2 Introduction

Adaptive Body Biasing (ABB) dynamically adjusts the threshold voltage (V_{TH}) of MOSFETs to optimize performance and compensate for Process, Voltage, and Temperature

(PVT) variations. This research explores ABB implementation in equalizers, focusing on:

1. Continuous-Time Linear Equalizers (CTLEs).
2. Decision Feedback Equalizers (DFEs).
3. Feed Forward Equalizers (FFEs).

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3 Objectives

1. Design equalizers (CTLE, DFE, or FFE) with ABB for enhanced performance.
2. Develop a Closed-Loop Controller for PVT compensation and circuit optimization.

4 Design and Implementation

4.1 Equalizer Design

1. **CTLE:** A 1st or 2nd-order analog equalizer for high-frequency compensation using ABB.
2. **DFE:** Combines ABB for dynamic feedback adjustments and ISI reduction.
3. **FFE:** Uses ABB for real-time tap coefficient adaptation in pre-compensation.

4.2 Closed-Loop Controller

A digital feedback system(preferably in System-Verilog) monitors circuit performance and dynamically adjusts ABB to optimize performance under varying PVT conditions.

5 Testbench Development and Analysis

1. **Testbench Design:** Verify functionality under nominal and varied PVT conditions.
2. **Simulation Results:** Perform Corner and Monte Carlo analyses to evaluate:
   - Performance metrics (gain, bandwidth, noise figure).
   - ABB effectiveness in compensating PVT variations.

6 Report and Presentation

1. Prepare a comprehensive report in LaTeX covering all aspects of design and results.
2. Deliver a presentation (preferably in English) to a small audience, explaining ABB integration and performance outcomes.