Semi-Automated Analog Layout Generation Using Cadence SKILL and Parameterized Cells (PCells)

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1 Description

Custom analog layout is traditionally a manual process requiring skilled designers to ensure matching, symmetry, and layout efficiency. This work proposes a semi-automated layout generation flow leveraging the Cadence Virtuoso Design Environment with SKILL scripting and PCells (Parameterized Cells). The proposed method aims to speed up layout generation while maintaining high design quality and layout compliance.

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2 Introduction

Analog layout automation still lags far behind digital synthesis due to complex device matching requirements and layout-dependent effects. The SKILL language in Cadence Virtuoso offers programmable layout generation capabilities. By using parameterized cells (PCells), one can generate reusable and scalable layout templates. This master thesis aims to integrate a SKILL-based layout framework to streamline analog building block layout generation.

Target Technologies: The developed methodology will primarily focus on higher node technologies such as **GlobalFoundries 22nm FDSOI** and/or **GF12nm FinFET**, enabling compatibility with modern analog/mixed-signal IC design platforms.

3 Objectives

1. Develop a reusable PCell library for key analog primitives: MOSFETs, resistors, capacitors.
2. Implement SKILL scripts to automate parameter-driven layout generation.
3. Create layout constraints such as symmetry, alignment, and spacing rules.
4. Validate generated layouts via DRC and LVS.

4 Design and Implementation

4.1 PCell Creation and CDF

Each PCell encapsulates a basic circuit element (e.g., transistor array), with parameters like width, length, number of fingers, and guard rings.

- SKILL code defines shapes and layout instances.

- CDF (Component Description Format) integrates parameters into the user interface.
- Callbacks and constraints ensure correct and DRC-clean layouts.

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4.2 Semi-Automated Layout Flow

1. Generate PCells via SKILL scripts.
2. Assemble layouts using SKILL-based templates for higher-order cells.
3. Integrate symmetry-aware placement rules and routing templates.

5 Testbench Development and Analysis

- Use Cadence Virtuoso and Calibre for DRC and LVS.
- Validate the layout under parameter sweeps.
- Compare semi-automated layouts with manually designed counterparts for:
  - Area efficiency
  - Time-to-layout
  - Matching quality

6 Scope Flexibility and Collaboration

The scope of the thesis can be tailored based on the student's background and interest. Potential extensions include:

- Integration of **Python-based layout scripting** or data-driven layout generation.
- Extension to additional devices or layout methodologies.
- Collaboration with ongoing research in layout automation.

Students with a strong interest in analog IC design, layout automation, or scripting are encouraged to apply.

7 Report and Presentation

- Documentation of SKILL code, methodology, and layout screenshots including a detailed master thesis report.
- Presentation to peers (preferably in English) and faculty of IES demonstrating layout workflow and results.