Module name					
Logic Design					
Module nr. 18-hb-1010	**Credit points** 6 CP	**Workload** 180 h	**Self study** 120 h	**Module duration** 1 Term	**Module cycle** Winter term
Language German			**Module owner** Prof. Dr.-Ing. Christian Hochberger		

1	**Teaching content** Boolean algebra, logic gates, hardware description languages, flipflops, sequential circuits, state-diagrams and -tables, technology mapping, programmable logic circuits
2	**Learning objectives** By this module, Students will be enabled to • rewrite boolean expressions and transform them into circuits of logic gates • analyze and synthesize digital circuits • describe digital circuits in a hardware description language • extract finite state machines from informal descriptions and implement them with synchronous circuits
3	**Prerequisite for participation**
4	**Form of examination** Module exam: • Module exam (Technical examination, Examination, Duration: 90 min, Default RS)
5	**Prerequisite for the award of credit points** Passing the final module examination
6	**Grading** Module exam: • Module exam (Technical examination, Examination, Weighting: 100 %)
7	**Usability of the module** B.Sc. etit, B.Sc. MEC
8	**Grade bonus compliant to §25 (2)**
9	**References** R.H. Katz: Contemporary Logic Design

Courses

	Course Nr. 18-hb-1010-vl	**Course name** Logic Design		
	Instructor M. Sc. Alexander SchwarzProf. Dr.-Ing. Christian Hochberger		**Type** Lecture	**SWS** 3
	Course Nr. 18-hb-1010-ue	**Course name** Logic Design		
	Instructor M. Sc. Alexander SchwarzProf. Dr.-Ing. Christian Hochberger		**Type** Practice	**SWS** 1